REMARKS

In the non-final Office Action, the Examiner rejected claims 1-61 under 35 U.S.C. § 102(e) as anticipated by Zhang et al. (U.S. Patent No. 6,795,506).

By this Amendment, Applicants amend the title to improve form; cancel claims 58 and 60 without prejudice or disclaimer; amend claims 1, 4, 5, 10, 11, 19-21, 23, 24, 29, 30, 38, 39, 56, 57, 59, and 61 to improve form; and add new claims 62 and 63. Applicants respectfully traverse the Examiner's rejection under 35 U.S.C. § 102 with regard to the claims as presented herein. Claims 1-57, 59, and 61-63 are pending.

In paragraphs 1-25 of the Office Action, the Examiner rejected pending claims 1-57, 59, and 61 under 35 U.S.C. § 102(e) as allegedly anticipated by Zhang et al. Applicants respectfully traverse the rejection.

A proper rejection under 35 U.S.C. § 102 requires that a single reference teach every aspect of the claimed invention. Any feature not directly taught must be inherently present. In other words, the identical invention must be shown in as complete detail as contained in the claim. See M.P.E.P. § 2131. Zhang et al. does not disclose or suggest the combination of features recited in claims 1-57, 59, and 61.

Amended independent claim 1, for example, is directed to a system comprising a memory configured to store data associated with a plurality of incoming streams of different speeds; an interface controller comprising a first arbitration element to arbitrate among the streams to store the data in the memory, the first arbitration element including a number of first entries, one of the first entries indicating which of the streams is to be serviced in a particular first time slot, the streams being assigned to the first entries based on the speeds of the streams; and a dispatch unit

comprising a second arbitration element to arbitrate among the streams to read the data from the memory, the second arbitration element including a number of second entries, one of the second entries indicating which of the streams is to be serviced in a particular second time slot, the streams being assigned to the second entries based on the speeds of the streams.

Zhang et al. does not disclose or suggest the combination of features recited in amended claim 1. For example, Zhang et al. does not disclose or suggest an interface controller that comprises a first arbitration element to arbitrate among a plurality of streams of different speeds to store data in a memory, where the first arbitration element includes a number of first entries, one of the first entries indicates which of the streams is to be serviced in a particular first time slot, and the streams are assigned to the first entries based on the speeds of the streams.

The Examiner alleged that Zhang et al. discloses a first arbitration element that is configured to store a plurality of entries and that the number of entries for a particular one of the streams is based on a speed of the stream and cited column 21, lines 52-67, of Zhang et al. for support (Office Action, paragraphs 5 and 6). Without acquiescing in the Examiner's allegations, Applicants submit that Zhang et al. does not disclose or remotely suggest an interface controller that comprises a first arbitration element to arbitrate among a plurality of streams of different speeds to store data in the memory, where the first arbitration element includes a number of first entries, one of the first entries indicates which of the streams is to be serviced in a particular first time slot, and the streams are assigned to the first entries based on the speeds of the streams, as required by claim 1.

At column 21, line 52 - column 22, line 1, Zhang et al. discloses:

> The rate controller 409 connects to both the bit rate converter apparatus 406 and the scheduler 411 and determines what bit rate is to be used for each input compressed

> bitstream. More specifically, based on messages received from the rate controller 409, the bit rate converter apparatus 406 adjusts the bit rate for each compressed bitstream. In one embodiment, the objective of the rate controller 409 is to determine whether to apply more aggressive transcoding and bit rate conversion to a particular compressed bitstream and use the saved bandwidth resulting therefrom for a different compressed bitstream. In a statistical re-multiplexing environment for example, if a particular compressed bitstream is encoded with fewer number of bits, then the remaining compressed bitstreams in the multiplex will be able to use more bits, resulting in a quality trade-off between different compressed bitstreams via bandwidth re-allocation.

In this section, Zhang et al. discloses a bit rate converter apparatus 406 that adjusts the bit rate for each compressed bitstream so that saved bandwidth can be used for a different compressed bitstream. Nowhere in this section does Zhang et al. disclose anything similar to a first arbitration element that includes a number of entries, let alone, an interface controller that comprises a first arbitration element to arbitrate among a plurality of streams of different speeds to store data in the memory, where the first arbitration element includes a number of first entries, one of the first entries indicates which of the streams is to be serviced in a particular first time slot, and the streams are assigned to the first entries based on the speeds of the streams, as required by claim 1.

Zhang et al. also does not disclose or suggest a dispatch unit that comprises a second arbitration element to arbitrate among the streams to read the data from the memory, where the second arbitration element includes a number of second entries, one of the second entries indicates which of the streams is to be serviced in a particular second time slot, and the streams are assigned to the second entries based on the speeds of the streams, as further recited in amended claim 1.

The Examiner alleged that Zhang et al. discloses a second arbitration element that is configured to store a plurality of entries and that the number of entries for a particular one of the

streams is based on a speed of the stream and cited column 21, lines 52-67, of Zhang et al. for support (Office Action, paragraphs 11 and 12). Without acquiescing in the Examiner's allegations, Applicants submit that Zhang et al. does not disclose or remotely suggest a dispatch unit that comprises a second arbitration element to arbitrate among the streams to read the data from the memory, where the second arbitration element includes a number of second entries, one of the second entries indicates which of the streams is to be serviced in a particular second time slot, and the streams are assigned to the second entries based on the speeds of the streams, as further recited in claim 1.

Column 21, line 52 - column 22, line 1, of Zhang et al. is reproduced above. In this section, Zhang et al. discloses a bit rate converter apparatus 406 that adjusts the bit rate for each compressed bitstream so that saved bandwidth can be used for a different compressed bitstream. Nowhere in this section does Zhang et al. disclose or remotely suggest a second arbitration element that includes a number of second entries, let alone a dispatch unit that comprises a second arbitration element to arbitrate among the streams to read the data from the memory, where the second arbitration element includes a number of second entries, one of the second entries indicates which of the streams is to be serviced in a particular second time slot, and the streams are assigned to the second entries based on the speeds of the streams, as required by claim 1.

For at least these reasons, Applicants submit that claim 1 is not anticipated by Zhang et al. Claims 2-20 and 59 depend from claim 1 and are, therefore, not anticipated by Zhang et al. for at least the reasons given with regard to claim 1. Claims 2-20 and 59 are also not anticipated by Zhang et al. for reasons of their own.

For example, claim 2 recites that the memory includes a plurality of memory buckets corresponding to the streams. Zhang et al. does not disclose or suggest this feature. The Examiner alleged that Zhang et al. discloses this feature and cited column 28, line 65 - column 29, line 3, of Zhang et al. for support (Office Action, paragraph 3). Applicants disagree.

At column 28, line 64 - column 29, line 3, Zhang et al. discloses:

> In an alternative embodiment, processor 863 is specially designed hardware for controlling the operations of router 810. In a preferred embodiment, a memory 861 (such as non-volatile RAM and/or ROM) also forms part of CPU 862. However, there are many different ways in which memory could be coupled to the system.

In this section, Zhang et al. discloses that CPU 862 includes a memory 861 that may take the form of non-volatile RAM and/or ROM. Even assuming, for the sake of argument, that memory 861 can be equated to a memory configured to store data associated with a plurality of incoming streams of different speeds (a point that Applicants do not concede), Zhang et al. does not disclose or remotely suggest that memory 861 includes a plurality of memory buckets corresponding to the plurality of streams of different speeds, as required by claim 2.

For at least these additional reasons, Applicants submit that claim 2 is not anticipated by Zhang et al. Claim 3 depends from claim 2 and is, therefore, also not anticipated by Zhang et al. for at least the reasons given with regard to claim 2.

Claim 4 recites that each of the first entries includes a stream number that identifies one of the streams. Zhang et al. does not disclose or suggest this feature. The Examiner alleged that Zhang et al. discloses this features and cited column 21, lines 52-67, of Zhang et al. for support (Office Action, paragraph 5). Applicants disagree.

Column 21, line 52 - column 22, line 1, of Zhang et al. is reproduced above. In this section, Zhang et al. discloses a bit rate converter apparatus 406 that adjusts the bit rate for each

compressed bitstream so that saved bandwidth can be used for a different compressed bitstream. Nowhere in this section, or elsewhere, does Zhang et al. disclose or remotely suggest each of a plurality of first entries that includes a stream number that identifies one of the streams, as required by claim 4.

For at least these additional reasons, Applicants submit that claim 4 is not anticipated by Zhang et al. Claims 6-8 depend from claim 4 and are, therefore, also not anticipated by Zhang et al. for at least the reasons given with regard to claim 4.

Claim 5 recites that the number of the first entries in the first arbitration element is programmable. Zhang et al. does not disclose or remotely suggest this feature.

For at least these additional reasons, Applicants submit that claim 5 is not anticipated by Zhang et al.

Claim 9 recites that the first and second arbitration elements are synchronized. Zhang et al. does not disclose or suggest this feature. The Examiner alleged that Zhang et al. discloses this feature and cited column 19, lines 41-54, of Zhang et al. for support (Office Action, paragraph 10). Applicants disagree.

At column 19, lines 41-55, Zhang et al. discloses:

> In order to effectively extract and use the bit rate information, it is synchronized with a compressed elementary stream by the encoding multiplexer, e.g. the scheduler 66 of FIG. 3C in a timely manner. In one embodiment, the bit rate information is inserted prior to the start of the access unit it is associated with More specifically, it is inserted just before the picture_start_code of the associated access unit, but not before the picture_start_code of the previous access_unit.
>
> FIG. 4C illustrates the insertion of a transport packet 360 containing the bit rate information 302a into a transport stream 362 according to one embodiment of the present invention. The transport stream 362 includes three transport packets 364, 366 and 368 that contain packetized data from access unit (N-1) 370 and access unit (N) 372.

In this section, Zhang et al. discloses that the encoding multiplexer (e.g., scheduler 66) synchronizes the bit rate information with a compressed elementary stream. Nowhere in this section, or elsewhere, does Zhang et al. disclose or suggest a first arbitration element or a second arbitration element, as recited in claim 1, let alone first and second arbitration elements that are synchronized, as required by claim 9. Synchronization of bit rate information with a compressed elementary stream cannot reasonably be equated to first and second arbitration elements that are synchronized, as required by claim 9.

For at least these additional reasons, Applicants submit that claim 9 is not anticipated by Zhang et al.

Claim 10 recites that each of the second entries includes a stream number that identifies one of the streams. Zhang et al. does not disclose or suggest this feature. The Examiner alleged that Zhang et al. discloses this feature and cited column 21, lines 52-67, of Zhang et al. for support (Office Action, paragraph 11). Applicants disagree.

Column 21, line 52 - column 22, line 1, of Zhang et al. is reproduced above. In this section, Zhang et al. discloses a bit rate converter apparatus 406 that adjusts the bit rate for each compressed bitstream so that saved bandwidth can be used for a different compressed bitstream. Nowhere in this section, or elsewhere, does Zhang et al. disclose or remotely suggest each of a plurality of second entries that includes a stream number that identifies one of the streams, as required by claim 10.

For at least these additional reasons, Applicants submit that claim 10 is not anticipated by Zhang et al. Claim 12 depends from claim 10 and is, therefore, also not anticipated by Zhang et al. for at least the reasons given with regard to claim 10.

Claim 11 recites that the number of the second entries in the second arbitration element is programmable. Zhang et al. does not disclose or remotely suggest this feature.

For at least these additional reasons, Applicants submit that claim 11 is not anticipated by Zhang et al.

Claim 13 recites flow control logic configured to initiate flow control on the storing of data in the memory. Zhang et al. does not disclose or suggest this feature. The Examiner alleged that Zhang et al. discloses this feature and cited column 21, lines 52-67, of Zhang et al. for support (Office Action, paragraph 14). Applicants disagree.

Column 21, line 52 - column 22, line 1, of Zhang et al. is reproduced above. In this section, Zhang et al. discloses a bit rate converter apparatus 406 that adjusts the bit rate for each compressed bitstream so that saved bandwidth can be used for a different compressed bitstream. Nowhere in this section does Zhang et al. disclose a memory configured to store data associated with a plurality of incoming streams of different speeds and, therefore, Zhang et al. cannot disclose or suggest flow control logic configured to initiate flow control on the storing of data in the memory, as required by claim 13.

The Examiner relied on column 29, lines 49-57, as allegedly disclosing the memory (Office Action, paragraph 1). At column 29, lines 49-57, Zhang et al. discloses that the network device "may employ one or more memories or memory modules . . . [that] may also be configured to store data streams." Assuming, for the sake of argument, that these one or more memories or memory modules can be equated to a memory configured to store data associated with a plurality of incoming streams of different speeds (a point that Applicants do not concede), nowhere does Zhang et al. disclose or remotely suggest that bit rate converter apparatus 406, or

any of the other elements shown in Fig. 5A, is configured to initiate flow control on the storing of data in the memory, as would be required by claim 13.

For at least these additional reasons, Applicants submit that claim 13 is not anticipated by Zhang et al. Claims 14-18 depend from claim 13 and are, therefore, also not anticipated by Zhang et al. for at least the reasons given with regard to claim 13.

Claim 19 recites that each of the streams has an associated watermark for performing flow control on the storing of data in the memory. Zhang et al. does not disclose or suggest this feature. The Examiner alleged that Zhang et al. discloses this feature and cited column 21, lines 45-51, of Zhang et al. for support (Office Action, paragraph 20). Applicants disagree.

At column 21, lines 45-51, Zhang et al. discloses:

> The multiplexer 408 also includes the rate controller 409 and a set of multiple input buffers 407. The input buffers 407 temporarily store compressed video data received from the transcoder 406 for each of the input compressed bitstreams until the scheduler 411 processes the compressed video data for transmission. In one embodiment, the multiplexer 408 is an open loop multiplexer.

In this section, Zhang et al. discloses input buffers that temporarily store compressed video data for each of the input compressed bitstreams until scheduler 411 processes the compressed video data for transmission. Nowhere in this section does Zhang et al. disclose or suggest each of a plurality of streams that has an associated watermark for performing flow control on the storing of data in memory, as required by claim 19.

For at least these additional reasons, Applicants submit that claim 19 is not anticipated by Zhang et al.

Claim 20 recites that each of the streams has two associated watermarks for performing flow control on the storing of data in the memory. Zhang et al. does not disclose or suggest this

feature. The Examiner alleged that Zhang et al. discloses this feature and cited column 21, lines 45-51, of Zhang et al. for support (Office Action, paragraph 21). Applicants disagree.

Column 21, lines 45-51, of Zhang et al. is reproduced above. In this section, Zhang et al. discloses input buffers that temporarily store compressed video data for each of the input compressed bitstreams until scheduler 411 processes the compressed video data for transmission. Nowhere in this section does Zhang et al. disclose or suggest each of a plurality of streams that has two associated watermarks for performing flow control on the storing of data in memory, as required by claim 20.

For at least these additional reasons, Applicants submit that claim 20 is not anticipated by Zhang et al.

Claim 59 recites that at least one of the first arbitration element or the second arbitration element is configured to be reprogrammed when the speed of one of the streams changes. Zhang et al. does not disclose or remotely suggest this feature.

The Examiner alleged that Zhang et al. discloses at least one of the first arbitration element or the second arbitration element that is configured to be reprogrammed based on an input regarding a speed of at least one of the streams and cited column 28, lines 6-19, of Zhang et al. for support (Office Action, paragraph 25). Without acquiescing in the Examiner's allegation, Applicants submit that Zhang et al. does not disclose or suggest at least one of the first arbitration element or the second arbitration element that is configured to be reprogrammed when the speed of one of the streams changes, as recited in claim 59.

At column 28, lines 6-19, Zhang et al. discloses:

> While the compressed bitstreams are stored, one or more are retrieved for off-line processing 706. Off-line processing 706 comprises decoding by a decoder 708, encoding

> by an encoder 712, and generation of the bit rate information by a processing apparatus 714, either while the data is uncompressed or during compression by the encoder 712. The processing apparatus 714 outputs the bit rate information to a combiner 716 that embeds the bit rate information in the compressed bitstream to form a modified compressed bitstream. The output compressed bitstream comprising the video data and the bit rate information are then stored in memory 704. From this point, the modified compressed bitstream may be transmitted or multicast as desired.

In this section, Zhang et al. discloses that bit rate information is embedded in a compressed bitstream to form a modified compressed bitstream. Nowhere in this section, or elsewhere, does Zhang et al. disclose or suggest a first or second arbitration element, let alone at least one of a first arbitration element or a second arbitration element that is configured to be reprogrammed when the speed of one of the streams changes, as required by claim 59.

For at least these additional reasons, Applicants submit that claim 59 is not anticipated by Zhang et al.

Amended independent claim 21 is directed to a method comprising storing data from a plurality of streams of potentially different speeds in a memory using a first arbitration scheme that stores data associated with a faster one of the streams in the memory at a higher rate than data associated with a slower one of the streams; and reading the data from the memory using a second arbitration scheme that reads the data associated with the faster one of the streams from the memory at a higher rate than the data associated with the slower one of the streams.

Zhang et al. does not disclose or suggest the combination of features recited in claim 21. For example, Zhang et al. does not disclose or suggest storing data from a plurality of streams of potentially different speeds in a memory using a first arbitration scheme that stores data associated with a faster one of the streams in the memory at a higher rate than data associated with a slower one of the streams. Zhang et al. simply discloses nothing similar to these features.

Zhang et al. also does not disclose or suggest reading the data from the memory using a second arbitration scheme that reads the data associated with the faster one of the streams from the memory at a higher rate than the data associated with the slower one of the streams, as further recited in claim 21. Zhang et al. simply discloses nothing similar to these features either.

For at least these reasons, Applicants submit that claim 21 is not anticipated by Zhang et al. Claims 22-39 and 61 depend from claim 21 and are, therefore, not anticipated by Zhang et al. for at least the reasons given with regard to claim 21. Claims 22-39 and 61 also recite features similar to, but possibly different in scope from, features recited in claims 2-20 and 59. Claims 22-39 and 61 are, therefore, also not anticipated by Zhang et al. for at least reasons similar to reasons given with regard to claims 2-20 and 59.

Independent claim 40 is directed to a system for performing flow control on data in a plurality of incoming streams of variable speeds. The system comprises a buffer configured to temporarily store data from a plurality of streams of variable speeds in a plurality of entries, a counter configured to determine a number of entries in the buffer corresponding to each of the streams, and a comparator configured to determine whether to initiate flow control for each of the streams based on the determined number of entries for the stream.

Zhang et al. does not disclose or suggest the combination of features recited in claim 40. For example, Zhang et al. does not disclose or suggest a counter that is configured to determine a number of entries in the buffer corresponding to each of the streams of variable speeds. The Examiner did not specifically address this feature of claim 40. Therefore, the Examiner did not establish a proper case of anticipation with regard to claim 40.

When rejecting a feature in claim 16, however, the Examiner alleged that Zhang et al. discloses a counter that is configured to determine a number of entries in a buffer corresponding to each of the streams and cited column 29, lines 49-57, of Zhang et al. for support (Office Action, paragraph 17). Applicants respectfully disagree.

At column 29, lines 49-57, Zhang et al. discloses that the network device "may employ one or more memories or memory modules . . . [that] may also be configured to store data streams." Assuming, for the sake of argument, that these one or more memories or memory modules can be equated to a buffer configured to temporarily store data from a plurality of streams of variable speeds in a plurality of entries (a point that Applicants do not concede), nowhere does Zhang et al. disclose or remotely suggest a counter that is configured to determine a number of entries in the buffer corresponding to each of the streams of variable speeds, as required by claim 40.

Zhang et al. also does not disclose or suggest a comparator configured to determine whether to initiate flow control for each of the streams based on the determined number of entries for the stream, as further recited in claim 40. The Examiner did not specifically address this feature of claim 40. Therefore, the Examiner did not establish a proper case of anticipation with regard to claim 40.

When rejecting a feature in claim 16, however, the Examiner alleged that Zhang et al. discloses a comparator configured to determine whether to initiate flow control for each of the streams based on the determined number of entries for the stream and cited column 21, lines 52-67, of Zhang et al. for support (Office Action, paragraph 17). Applicants respectfully disagree.

Column 21, lines 52-67, of Zhang et al. is reproduced above. In this section, Zhang et al. discloses a bit rate converter apparatus 406 that adjusts the bit rate for each compressed bitstream so that saved bandwidth can be used for a different compressed bitstream. Nowhere in this section, or elsewhere, does Zhang et al. disclose or suggest a comparator configured to determine whether to initiate flow control for each of the streams of variable speeds based on the determined number of entries for the stream, as required by claim 40.

For at least these reasons, Applicants submit that claim 40 is not anticipated by Zhang et al. Claims 41-47 depend from claim 40 and are, therefore, not anticipated by Zhang et al. for at least the reasons given with regard to claim 40.

Independent claims 48 and 55 recite features similar to, but possibly different in scope from, features recited in claim 40. Claims 48 and 55 are, therefore, not anticipated by Zhang et al. for at least reasons similar to reasons given with regard to claim 40. Claims 49-54 depend from claim 48 and are, therefore, not anticipated by Zhang et al. for at least the reasons given with regard to claim 48.

Amended independent claim 56 is directed to a network device that comprises an input interface configured to receive a plurality of packets belonging to a plurality of streams of differing speeds, access a first arbitration scheme that services a faster one of the streams more often than a slower one of the streams, and output the packets based on the first arbitration scheme; input logic comprising flow control logic configured to initiate flow control on the packets output by the input interface, a memory configured to store the packets from the input interface, and a dispatch unit configured to access a second arbitration scheme that services the faster one of the streams more often than the slower one of the streams, and read the packets

from the memory based on the second arbitration scheme; and one or more packet processors configured to process the packets from the dispatch unit.

Zhang et al. does not disclose or suggest the combination of features recited in claim 56. For example, Zhang et al. does not disclose or suggest an input interface configured to, among other things, access a first arbitration scheme that services a faster one of the streams more often than a slower one of the streams and output packets based on the first arbitration scheme, for at least reasons similar to reasons given with regard to claim 21.

Zhang et al. also does not disclose or suggest a dispatch unit configured to access a second arbitration scheme that services the faster one of the streams more often than the slower one of the streams, and read packets from the memory based on the second arbitration scheme, as further recited in claim 56, for at least reasons similar to reasons given with regard to claim 21.

For at least these reasons, Applicants submit that claim 56 is not anticipated by Zhang et al.

Amended independent claim 57 is directed to a network device that comprises means for receiving a plurality of packets belonging to a plurality of streams of potentially different speeds; means for storing the packets based on a first arbitration scheme that stores the packets based on the speeds of the streams to which the packets belong; means for performing flow control on the storing of the packets; means for reading the packets based on a second arbitration scheme that reads the packets based on the speeds of the streams to which the packets belong; and means for processing the packets read based on the second arbitration scheme.

Zhang et al. does not disclose or suggest the combination of features recited in claim 57. For example, Zhang et al. does not disclose or suggest means for storing the packets based on a first arbitration scheme that stores the packets based on the speeds of the streams to which the packets belong.

The Examiner alleged that Zhang et al. discloses a first arbitration element that is configured to arbitrate among streams of variable speeds to store data in a memory based on the speeds of the streams and cited column 20, lines 40-48, of Zhang et al. for support (Office Action, paragraph 24). Without acquiescing in the Examiner's allegation, Applicants submit that Zhang et al. does not disclose or suggest means for storing the packets based on a first arbitration scheme that stores the packets based on the speeds of the streams to which the packets belong, as recited in claim 57.

At column 20, lines 40-48, Zhang et al. discloses:

> In one embodiment where the bit rate information is stored in a storage location of the compressed bitstream, the extractor apparatus 404 knows potential locations where the bit rate information may be stored, checks each location, and extracts the bit rate information from the storage location when found. The extractor apparatus 404 may also depacketize the bit rate information into data streams before outputting the bit rate information to the rate controller 409.

In this section, Zhang et al. discloses an extractor apparatus that knows potential locations where bit rate information may be stored, checks each location, and extracts the bit rate information from the storage location when found. Nowhere in this section, or elsewhere, does Zhang et al. disclose or suggest means for storing packets based on a first arbitration scheme that stores the packets based on the speeds of the streams to which the packets belong, as required by claim 57.

Zhang et al. also does not disclose or suggest means for reading the packets based on a second arbitration scheme that reads the packets based on the speeds of the streams to which the packets belong, as further recited in claim 57.

The Examiner alleged that Zhang et al. discloses a second arbitration element that is configured to arbitrate among streams of variable speeds to read data from a memory based on the speeds of the streams and cited column 20, lines 40-48, of Zhang et al. for support (Office Action, paragraph 24). Without acquiescing in the Examiner's allegation, Applicants submit that Zhang et al. does not disclose or suggest means for reading the packets based on a second arbitration scheme that reads the packets based on the speeds of the streams to which the packets belong, as recited in claim 57.

Column 20, lines 40-48, of Zhang et al. is reproduced above. In this section, Zhang et al. discloses an extractor apparatus that knows potential locations where bit rate information may be stored, checks each location, and extracts the bit rate information from the storage location when found. Nowhere in this section, or elsewhere, does Zhang et al. disclose or suggest means for reading the packets based on a second arbitration scheme that reads the packets based on the speeds of the streams to which the packets belong, as required by claim 57.

For at least these reasons, Applicants submit that claim 57 is not anticipated by Zhang et al.

New claim 62 depends from claim 59, and new claim 63 depends from claim 61. Claims 62 and 63 are, therefore, patentable over Zhang et al. for at least the reasons given with regard to claims 59 and 61.

In view of the foregoing amendments and remarks, Applicants respectfully request the Examiner's reconsideration of the application and the timely allowance of pending claims 1-57, 59, and 61-63.

As Applicants' remarks with respect to the Examiner's rejections are sufficient to overcome these rejections, Applicants' silence as to certain assertions by the Examiner in the Office Action or certain requirements that may be applicable to such rejections (e.g., whether a reference constitutes prior art, motivation to combine references, etc.) is not a concession by Applicants that such assertions are accurate or such requirements have been met, and Applicants reserve the right to analyze and dispute these assertions/requirements in the future.

If the Examiner does not believe that all pending claims are now in condition for allowance, the Examiner is urged to contact the undersigned to expedite prosecution of this application.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 50-1070 and please credit any excess fees to such deposit account.

Respectfully submitted,

HARRITY SNYDER, LLP

/Paul A. Harrity/
Paul A. Harrity
Reg. No. 39,574

Date: March 8, 2007

11350 Random Hills Road
Suite 600
Fairfax, Virginia 22030
(571) 432-0800